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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,374	12/12/2003	Betty Shu Mercer	TI-36853	1822

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
10/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/735,374	MERCER ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/30/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7,16,17,19-23 and 33-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 7, 16, 17, 19-23 and 33-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/20/200 has been entered.

Election/Restrictions

2. Applicant's election without traverse of claims 1-3, 7, 16, 17 and 19-23 in the reply filed on 06/27/2006 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7, 33 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Thomas et al. (US 5,117,276).

5. Regarding claim 1, Jeong (e.g. 3) shows an integrated circuit, comprising: a semiconductor substrate 21 comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer 23 comprising metal regions; a protective overcoat 27 formed over the metallization layers,

the protective overcoat having vias 37 through it; tungsten plugs 41 substantially filling the vias and connecting to one of the metal regions in the uppermost layer; and thick copper 45 formed over the protective overcoat and forming connections to the tungsten plugs (clm. 1 and 18). Although it is well known in the art the art that the uppermost layer (i.e. Jeong's 23) include multiple metal regions disposed between dielectric regions Jeong does not explicitly show it. However, Thomas (e.g. fig. 1K) shows an uppermost layer comprised by metal regions 108 disposed between dielectric regions (14, 15 & 30). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the uppermost layer disclosed by Jeong having multiple metal regions disposed between dielectric regions as suggested by Thomas to interconnect the plurality of electrical device formed on the semiconductor device.

6. Regarding claim 2, Jeong teaches that the uppermost layer is an aluminum metallization (col.3/lls. 9-10).

7. Regarding claims 3, Jeong teaches that the protective overcoat is made of silicon oxide (col. 4/lls. 60).

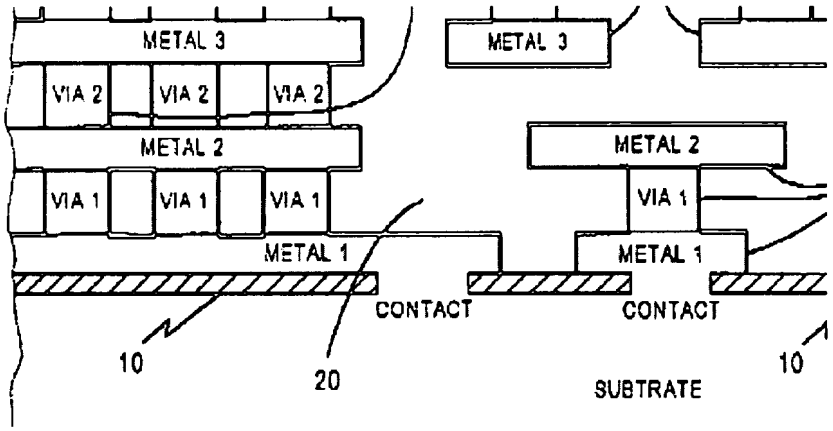
8. Regarding claims 7, Jeong teaches that the thick copper forms interconnections between device elements within the integrated circuit (col. 1/lls. 55-62).

9. Regarding claim 33, Jeong in view of Thomas show that the tungsten plug is electrically couple at leas one of the thick copper connections to one of the metal regions.

10. Regarding claim 34, Jeong in view of Thomas shows that the thick copper substantially overlies at least one of the metal regions.

11. Claims 16, 19-23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Buynoski (US 6,218,282).

12. Regarding claims 16 and 20, Jeong (e.g. fig. 3) shows an integrated circuit, comprising: a semiconductor substrate 21 comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer 23 comprising pads; a protective overcoat 27 formed over the metallization layers, the protective overcoat having vias 37 through it; wherein the array of vias are formed over individual bond pads, tungsten plugs 41 substantially filling the vias and connecting to the uppermost layer bond pads; and thick copper 45 formed over the protective overcoat and forming connections to the tungsten plugs (clm. 1 and 18). Jeong does not teaches that multiple vias are formed over individual bond pad. Nonetheless, Buynoski (e.g. fig. 4) shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1).



It would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple vias over individual bond pads disclosed by Jeong a suggested by Buynoski to increase device density and performance.

Regarding claim 19, Jeong teaches that the plug is made of tungsten with have a coefficient of thermal expansion less than or equal to about 8 ppm/C.

13. Regarding claim 21, Jeong teaches that the uppermost layer is an aluminum metallization (col.3/lls. 9-10).

14. Regarding claim 22, Jeong teaches that the protective overcoat is made of silicon oxide (col. 4/lls. 60).

15. Regarding claim 23, Jeong teaches that the thick copper forms interconnections between device elements within the integrated circuit (col. 1/lls. 55-62).

16. Regarding claim 36, Jeong in view of Buynoski shows that the multiple metal plugs individually couple the thick copper connection to the bond pads.

17. Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Buynoski (US 6,218,282) further in view of Ting et la. (US 5,969,422).

18. Regarding claim 17, Jeong in view of Buyoski discloses the claimed invention except for a plug made of copper. Ting teaches that copper is a suitable material for contact plugs (abstract, col. 6/lls. 10-15)). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the contact plug disclosed by Jeon in view of Buynoski of copper as suggested by Ting, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

19. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Thomas et al. (US 5,117,276) further in view of Or-Bach et al. (US 6,476,493).

20. Regarding claim 35, Jeong in view of Thomas teaches most aspects of the instant invention including a thick copper but does not explicitly teaches that the thick copper layer does not extend over at least a portion of the dielectric region. However, it is implicitly disclosed because metal interconnections are arranged as grid type array. Therefore, it is not possible for a layer to overlay the whole surface of the integrated circuit unless the layer is a metal plane. For example Or-Barch (e.g. fig. 3) shows the different interconnection metal levels interconnected by vias wherein an upper layer does not extend over the dielectric regions of a lower level (i.e. the space defined by at least two metal layers in the same level). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the thick copper layer such as to do not extend over at least a portion of the dielectric region disclosed by Jeong in view of Thomas to provide an interconnection system which has minimal parasitic capacitance and it is mechanically strong.

Response to Arguments

21. Applicant's arguments filed on 06/20/2007 have been considered but they are not persuasive. Applicant argues that Buynoski shows multiples vias formed over individual bond pads. Nevertheless, Buynoski (e.g. fig. 4) clearly shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1). The fact that the device includes bond pads 41 for external connection does not oppose in any way the

fact that multiples vias are formed over individual pads. Note that the contacts areas are recognized as pad.

22. Applicant argues "the proposed modification to Thomas (i.e., combining it with Jeong to obviate claim 1) would render Thomas unsatisfactory for its intended purpose. Therefore, there is no suggestion or motivation to make the proposed modification". However, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). The secondary reference was provided to show that it is well known in the art the art that the uppermost layer of an interconnection system in it is well known in the art the art that the uppermost layer include multiple metal regions disposed between dielectric regions. Note that the claim would have been obvious to because a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art see *KSR International Co. v. Teleflex Inc., 550 U.S.-, 82 USPQ2d 1385(2007).*

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leonardo Andujar
Primary Examiner
Art Unit 2826

9/24/2007